Low-k Interconnect Stack with Metal-Insulator-Metal Capacitors for 22nm High Volume Manufacturing

D. Ingerly, A. Agrawal, R. Ascazubi, A. Blattner, M. Buehler, V. Chikarmane, B. Choudhury, F. Cinnor, C. Ege, C. Ganpule, T. Glassman, R. Grover, P. Hentges, J. Hicks[1], D. Jones, A. Kandas, H. Khan, N. Lazo, K. S. Lee, H. Liu, A. Madhavan, R. McFadden, T. Mule', D. Parsons, P. Parthangal, S. Rangaraj[1], D. Rao, J. Roesler, A. Schmitz[1], M. Sharma, J. Shin, Y. Shusterman, N. Speer, P. Tiwari[2], G. Wang[2], P. Yashar, K. Mistry

Logic Technology Development, [1]Corporate Quality Network, [2]Assembly Test and Technology Development, Intel Corporation, 5200 NE Elam Young Pkwy, Hillsboro, OR 97229, USA.
doug.b.ingerly@intel.com

Abstract

We describe interconnect features for Intel's 22nm high-performance logic technology, with metal-insulator-metal capacitors and nine layers of interconnects. Metal-1 through Metal-6 feature a new ultra-low-k carbon doped oxide (CDO) and a low-k etch stop. Metal-7 and Metal-8 use a low-k CDO. New materials and process optimization provide 13-18% capacitance improvement. Single-exposure patterning for 80nm pitch layers makes the process cost-effective.

Introduction

This manuscript provides an overview of Intel's 22nm backend process with nine layers of interconnects (Figure 1). We scale our previously described interconnect stacks [1,2], and incorporate several improvements for increased performance, density, and reliability. We enable tighter pitches, more complex layout circuitry, and good end-to-end performance with the use of a dual exposure process at Metal-1. Metal-2 and Metal-3 use single-exposure patterning with 80nm pitch, which reduces the cost and complexity at these layers. For resistance and capacitance performance improvements, we introduce two new dielectric materials: ultra-low-k carbon doped oxide (CDO), and low-k etch stop (ES). The tightest via pitches are patterned using a self-aligned via (SAV) process with a sacrificial hard mask layer [2].

We also introduce metal-insulator-metal (MIM) capacitors integrated into the dielectric between Metal-8 and Metal-9, which are used for power supply and signal decoupling. A thick Metal-9 layer provides low-resistance power and signal routing, in addition to providing a mechanical buffer to package stresses [1].

Process Discussion

Metal-1–Metal-8 interconnects are patterned using the dual damascene process (Figure 1); the pitch for each layer is listed in Table 1. The lower layer (Metal-1 through Metal-6) patterning is done using SAV, with advantages as described in [2]. ES thicknesses have been aggressively scaled to 12nm, and ultra-low-k CDO is used at all SAV layers to decrease interconnect capacitance. The lower layers balance metal resistance and electromigration performance for reliable operation at the required current densities. Thinner barriers and new copper electroplating chemistries are used for good gapfill.

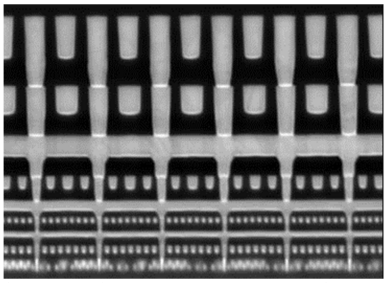

Figure 1: Metal-1–Metal-8 in cross-section, showing via and trench profiles.

Table 1: Pitch, thickness, and aspect ratio for the stack. (ULK CDO = ultra-low-k CDO; LK CDO = low-k CDO.)

Metal	Process	Dielectric	Pitch (nm)	Thickness (nm)	Aspect Ratio
1	SAV	ULK CDO	90	76	1.7
2	SAV	ULK CDO	80	68	1.7
3	SAV	ULK CDO	80	68	1.7
4	SAV	ULK CDO	112	110	2.0
5	SAV	ULK CDO	160	160	2.0
6	SAV	ULK CDO	240	240	2.0
7	Via First	LK CDO	320	310	1.9
8	Via First	LK CDO	360	468	2.6
9	Plate Up	Polymer	14µm	6µm	1.3

Metal-1 patterning uses dual exposure at trench patterning; this lithography scheme uses a grating/plug process which enables improved control of line end-to-end distances [3], and allows tighter design rules at Metal-1. For Metal-2 and Metal-3 we are able to robustly pattern the 80nm pitch using single exposure immersion lithography for both trench and via. We achieve excellent control of critical dimensions and end-to-end space while avoiding the more costly and complex dual exposure process (Figure 2).

Metal-7 and Metal-8 use a low-k CDO, in contrast to Intel's 32nm process, where Metal-8 used oxide. Both are patterned using a via-first approach, without the usage of a hard mask layer. Metal-8 has an aspect

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ratio of 2.6, significantly higher than other interconnect layers (Table 1). CDO at Metal-8 allows deeper trenches for lower resistance interconnects by providing improved interconnect capacitance.

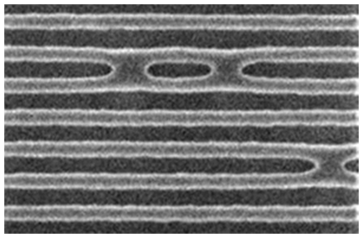

Figure 2: Metal-2 resist pattern.

Metal-insulator-metal (MIM) capacitors are embedded above Metal-8 in the silicon nitride dielectric between Metal-8 and Metal-9 (Figure 3). The capacitors are formed of an Hf-based high-k dielectric between two TiN electrodes. The electrodes are electrically connected to Via-8 through the Via-8 sidewalls. The MIM capacitors provide a capacitance density of >20fF/μm^2. This is the highest reported capacitance density for integrated MIM capacitors in high volume manufacturing. Via-8 and Metal-9 are patterned using a Cu plate-up process between sacrificial photoresist lines, followed by a spin coating of a polymer dielectric, as described in [1]. Figure 4 shows a cross-section of an assembled unit, with the solder, copper bump, and Metal-9 layer visible.

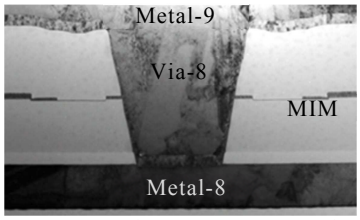

Figure 3: Transmission electron micrograph of Via-8, showing a MIM capacitor embedded in silicon nitride, and sidewall connections to the electrode.

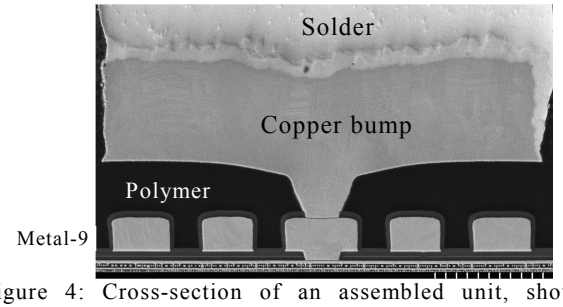

Figure 4: Cross-section of an assembled unit, showing solder, copper bump, and thick Metal-9 layer under bump.

Finally, the evolution of input-output and power pin density requirements resulting from scaling of backend and frontend features requires scaling the bump pitch. For the 22nm node, we scale the minimum bump pitch from 145μm (32nm) to 130μm. Low-k dielectric materials – and the use of low-k material further up the stack – in each new process node require substantial effort in reducing low-k dielectric stress for flip-chip assembly. Accordingly, we have optimized several backend (dielectric materials) and far-backend (stack thicknesses, critical dimensions, materials, material deposition parameters on both die and package) features to achieve 20% lower dielectric stress versus Intel's 32nm node (Figure 5).

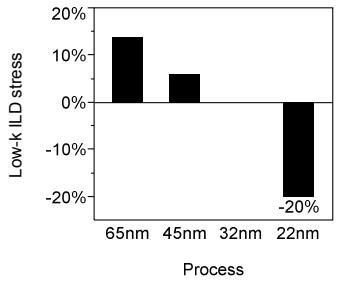

Figure 5: Post-packaging low-k dielectric stress for some recent Intel processes normalized to the 32nm node and measured at the uppermost low-k dielectric layer.

Results

The 22nm process delivers a minimum of 13% reduced capacitance at Metal-1 through Metal-6 relative to the 32nm technology generation at matched pitch (Figure 6). We do this by using an ultra-low-k CDO, increased via height, and a new ES film at the lower five metal layers. The new ultra-low-k CDO film provides lower dielectric constant at Metal-1–Metal-6. We optimized the properties for modulus, dielectric constant, and patterning. The etches are optimized to avoid excessive etch damage (impacts the k-value), and critical dimension loss. As shown in Figure 1, the final process has excellent via and trench profiles.

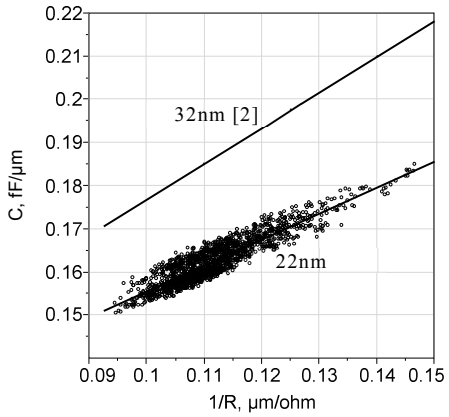

Figure 6: Capacitance, C, vs. inverse resistance, 1/R, at 112nm pitch (32nm: Metal-2; 22nm: Metal-4).

The ES film is scaled to 12nm (Figure 7), and the k-value is lowered by 18% versus Intel's 32nm process. The electromigration performance with the new ES is improved by >30% at matched thickness for the layers with the highest current densities.

Measured capacitance and resistance values for the 22nm process are shown in Figure 8 and Figure 9

at the Metal-2 and Metal-5 layers, respectively. We measure these for minimum pitch lines with 50% dense minimum-pitch metal patterns directly above and below the measured feature. The total capacitances are the sums of the line-to-line and layer-to-layer measured capacitances. The Metal-2 layer delivers 0.16fF/µm total capacitance and 21ohm/µm resistance at 80nm pitch (median values). The Metal-5 layer delivers 0.17fF/µm total capacitance and 2.8ohm/µm resistance at 160nm pitch (median values). Resistances at lower metal layers have a resistance penalty to enable higher current densities for high-performance logic. We optimized mid- and upper-layers for resistance due to lower electromigration requirements.

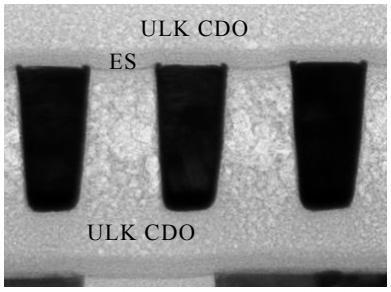

Figure 7: Transmission electron micrograph showing 12nm etch stop. The dark regions are copper interconnects.

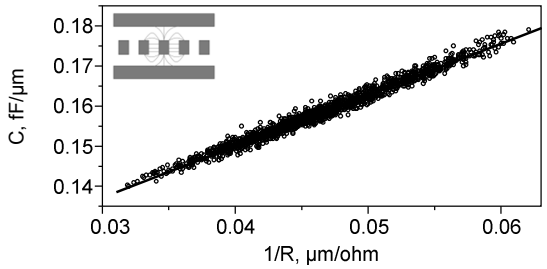

Figure 8: Capacitance, C, vs. inverse resistance, 1/R, Metal-2. The inset shows a schematic of the test structure.

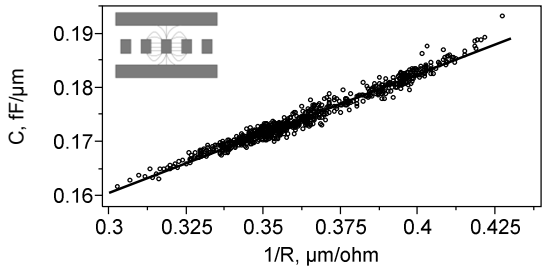

Figure 9: Capacitance vs. inverse resistance, Metal-5.

We noted previously that the low-k dielectric stresses had been reduced versus Intel's 32nm process. Doing so allows packaging without any low-k dielectric failures in high-volume manufacturing compatible volumes despite the use of lower-k dielectrics. In addition, we have completed standard humidity and temperature cycling tests without failure on several thousand units. Figure 10 shows a high-resolution confocal scanning acoustic microscope (CSAM) image of an early process version, where we observed massive area delamination on a significant fraction of units after a reliability stress (temperature cycling). Figure 11 shows representative images of 22nm microprocessor units after process optimization, before and after the same reliability stress, with no distinguishable regions of contrast caused by delamination. (Contrast variation across the images is a function of underlying layout.)

Figure 10: Early version of the process, with massive delamination from die edge after temperature cycling.

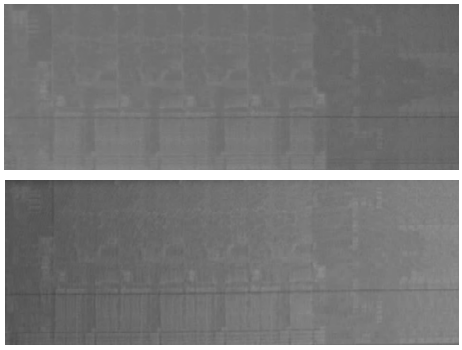

Figure 11: Final process, showing no delamination before (top) and after (bottom) temperature cycling.

Summary

We have implemented a new interconnect stack featuring ultra-low-k CDO, low-k ES, and MIM capacitors for Intel's 22nm node. The interconnect stack provides excellent resistance, capacitance, and reliability performance. Microprocessors using this interconnect stack are currently shipping in high-volume from multiple Intel fabrication facilities.

Acknowledgments

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References

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